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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,013	09/05/2003	Subhasish Mitra	ITL.0971US (P16171)	8151

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EXAMINER	
CHUNG, PHUNG M	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,013	MITRA ET AL.	
	Examiner	Art Unit	
	Phung My Chung	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/8/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 16 is rejected under 35 U.S.C. 112, first paragraph, as a single means or step claim (i.e., it recites a plurality of exclusive OR gates arranged to handle any number of scan chains with unknown logic values) recitation does not appear in combination with another recited elements of means or step. Thus, Claim 16 recites only a single means to cover every conceivable means for achieving the stated property, is subject to an undue breadth rejection under 35 U.S.C. 112, first paragraph. In re Hyatt, 708 F.2d, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983). (See MPEP 2164.08(a)).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 16 is rejected under 35 U.S.C. 102(e) as being anticipated by Mitra et al (2003/0188269).

As per claim 16, Mitra et al disclose a compacting circuit, comprising:

A plurality of exclusive OR gates arranged to handle any number of scan chains with unknown logic vales. (See Fig. 3 and paragraph (0016)).

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-15 and 17-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitra et al (2003/0188269).

As per claim 1, Mitra et al teach a compacting method, comprising:

Adding to a compactor the output that can produce unknown logic values at the same time. (See Fig. 2 and paragraph (0015)). Mitra et al do not disclose that adding at least two columns to a compactor matrix for each circuit output. However, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to add only

two columns of each circuit output to the compactor matrix instead of rows and columns. This is because Mitra et al do disclose adding output of each circuit including rows and columns to the compactor matrix and Mitra et al also disclose that any modification and variation are obvious to those skilled in the art. The advantage is to reduce the number of necessary pins or connectors can be reduced without increasing the size of the scan chains. (See paragraphs (0013 and 0015).

As per claim 2, Mitra et al further disclose that each circuit is a scan chain (paragraph 0013).

As per claims 3-8, Mitra et al further including obtaining the maximum number of scan chains that can produce unknown logic values at the same time. (See paragraphs (0015)-(0016)).

As per claim 9, Mitra et al teach a compacting method, comprising:

Obtaining a number of circuit outputs that can produce unknown logic values at the same time; and

Adding to a compactor the output that can produce unknown logic values at the same time. (See Fig. 2 and paragraph (0015)). Mitra et al do not disclose that adding at least two columns to a compactor matrix for each circuit output. However, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to add only two columns of each circuit output to the compactor matrix instead of rows and columns. This is because Mitra et al do disclose adding output of each circuit including rows and columns to the compactor matrix and Mitra et al also disclose that any modification and variation

are obvious to those skilled in the art. The advantage is to reduce the number of necessary pins or connectors can be reduced without increasing the size of the scan chains. (See paragraphs (0013 and 0015).

As per claims 10-15, these claims are rejected under similar rationale as set forth in claims 2-8.

As per claim 19, this claim is rejected under similar rationale as set forth in claims 1-2.

As per claims 20-25, these claims are also rejected under similar rationale as set forth in claims 3-8.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phung My Chung
Primary Patent Examiner
Art Unit 2138